AH743C

Two-wire differential wheel speed sensor (speed direction + AK protocol)

Alfa Electronics Co.,Ltd

1. Product Introduction

AH743C is a new generation wheel speed and direction detection sensor chip developed by Alfa Electronics Co. Ltd based on advanced differential Hall technology and high-performance, dedicated ASIC signal processor. The chip uses the AK protocol for dual line current interface communication, providing additional information such as rotation direction and air gap in addition to speed signals. This sensor does not require external components to operate and combines fast power on time with low cutoff frequency. Its excellent accuracy and sensitivity are suitable for demanding automotive requirements such as wide temperature range, high ESD, and EMC robustness.

Optimized piezoelectric compensation and integrated dynamic offset compensation improve the sensor's anti-interference ability against stray magnetic fields, ferromagnetic particles, or other disturbances.

AH743C also offers an external 1.8nF capacitor to enhance EMC performance.

2. Product Features

- AK communication protocol dual line current interface
- Wheel speed measurement
- Wheel rotation direction detection
- Air gap measurement
- Dynamic self calibration principle
- Single chip solution, no need for external components
- High sensitivity
- Back magnetic north and south pole self induction
- Large working air gap
- Wide working temperature range -40 ℃ ~150 ℃
- Wide working voltage range 6.5V~20V
- PG-SSO-2-4 package, RoHS certified

3. Application

- Anti-lock Braking System (ABS)
- Electronic Stability System (ESP)
- Automatic transmission
- Wheel speed sensing in automotive applications
- Other similar fields of wheel speed detection

Table of Contents

4. Product packaging

Part No.	operation temperature	Packages	Packing
AH743C	-40℃~150℃	PG-SSO-2-4	Braid, 1500 pieces/box

5. Naming convention

Part number AH743----C

① ②

①Series name ②C means built-in 1.8nF capacitor

6. Function Description

The AH743C circuit is powered internally by a 3V voltage regulator, and the on-chip oscillator serves as the clock generator for the DSP and output encoder. The AH742C signal path consists of a pair of Hall effect probes spaced 2.5mm apart, a differential amplifier with a noise limiting low-pass filter, and a comparator with a trigger switch current output stage. In addition, there are speed signal, direction signal tracking A/D converters, digital signal processors (DSPs), and offset cancellation D/A converters that provide offset cancellation feedback loops, as shown in Figure 6-1.

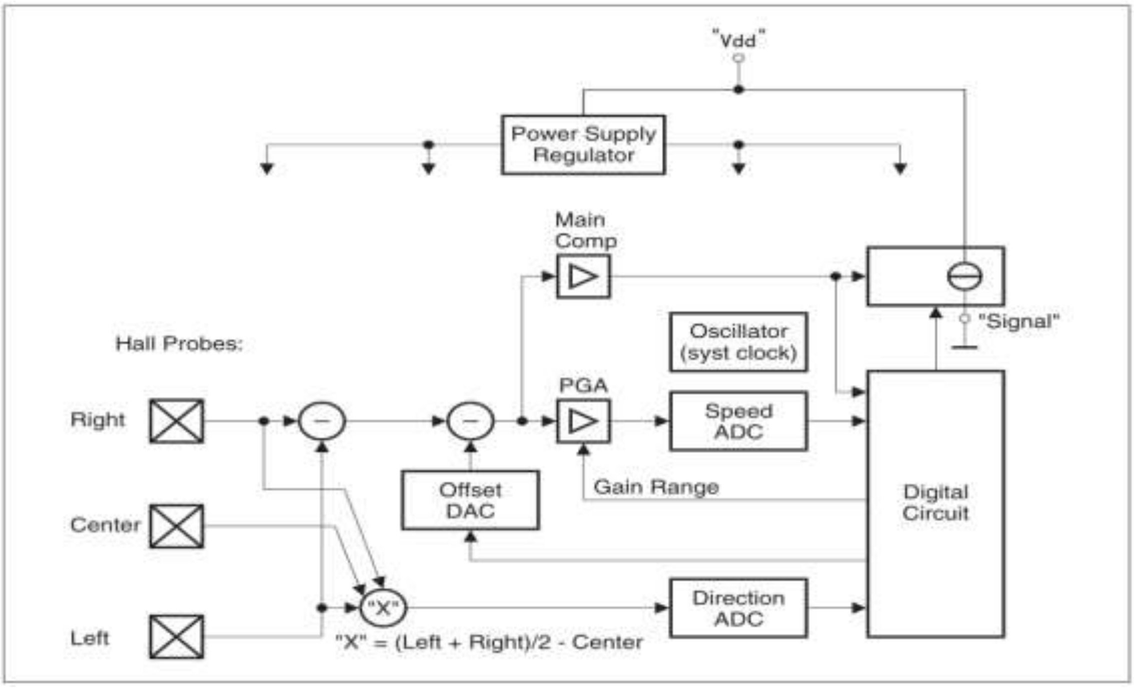


Figure 6-1: Functional block diagram

Differential Hall effect integrated circuits detect the motion of ferromagnetic or permanent magnetic structures by measuring the differential magnetic flux density of the magnetic field. In order to detect the motion of ferromagnetic objects, the magnetic field for detecting the motion of ferromagnetic objects (such as gears) must be provided by a back biased permanent magnet. The south or north pole of the magnet can be attached to the back of the IC package, on the unmarked side, as shown in Figure 6-2.

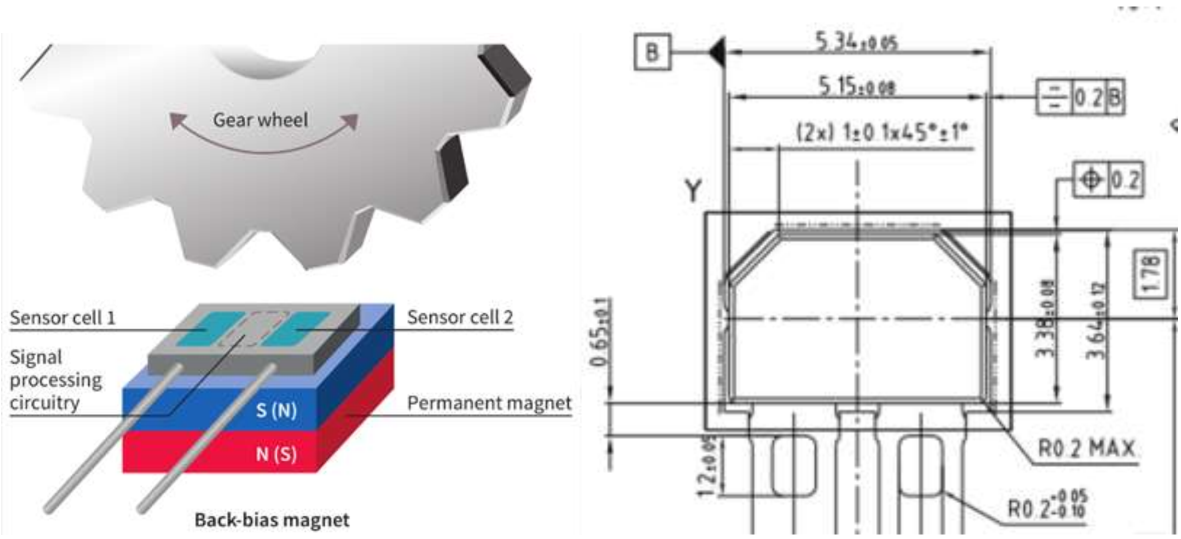


Figure 6-2 Sensor installation and sensing position

Magnetic offsets up to ±20mT are eliminated by a self-calibration algorithm, the self calibration process can be completed with only a few conversions. The left and right Hall elements generate a differential signal corresponding to the velocity of the detected object, and each zero crossing triggers an output pulse as shown in Figure 6-3; The directional signal is calculated by three Hall signals through a digital signal processor (DSP), and the data protocol is released and converted into a current modulation signal. This protocol consists of speed pulses emitted from zero crossing and other data bits determined by the DSP. The IC has a three-level current interface, corresponding to the AK protocol described in this data sheet.

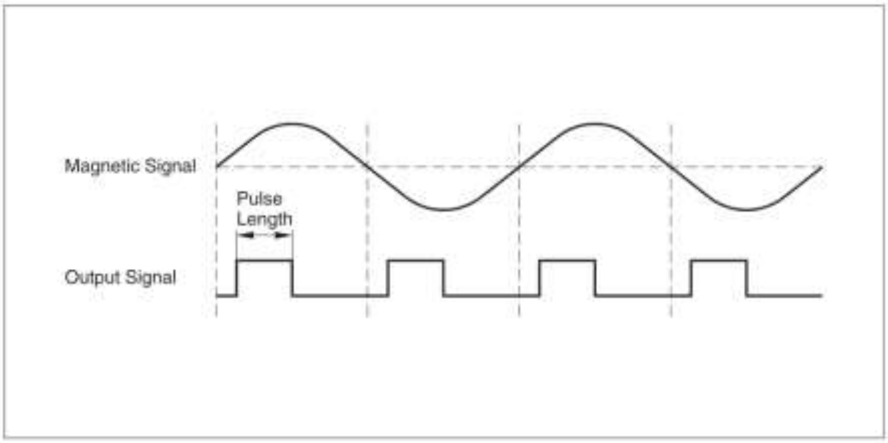


Figure 6-3 Zero crossing principle and corresponding pulse output

7. AK protocol description

The protocol consists of a speed pulse, a preset bit, and nine data information bits (data protocol) as shown in Figure 7-1.

The data protocol complies with Manchester coding rules. This means that the value of one bit is encoded between the mid current value (IMID) and low current value (ILOW) of the signal's rise or fall within a specific time window. '0' represents encoding from low to medium, '1' represents encoding from low to medium. Unused bits are output as default values. The falling and rising edges of the sensor output current are located in the middle position (tp/2) of the data protocol, as shown in Figure 7-2.

AK protocol data bit encoding specific information.

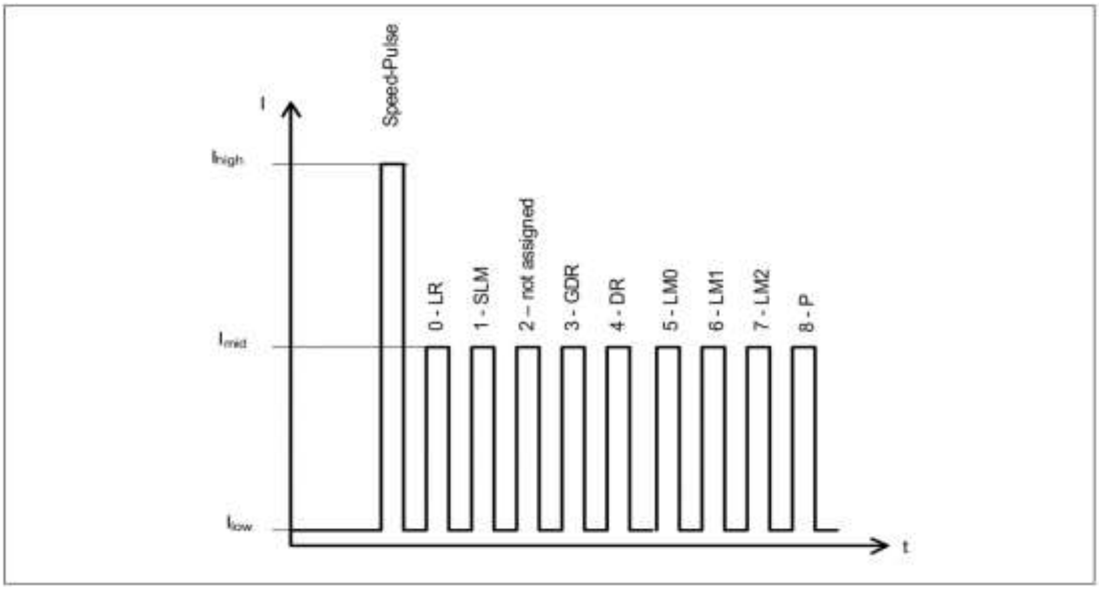


Figure 7-1 AK protocol data bit encoding

Bit#	Meaning	Name	Value (power on)）	Conditions
0	Air gap alarm	LR	0	If dB<dBLR alarm
1	Effectiveness of air gap measurement	SLM	1	'0' air gap measurement value is valid, '1' is invalid
2	undefined	NOP	0	
3	Directional effectiveness	GDR	0	'0' direction is invalid, '1' is valid
4	Rotation direction	DR	0	0 "positive direction CW" 1 "negative direction CCW
5	Low air gap measurement value	LM0	0	3-digit binary number (0~7)
6	Median value of air gap measurement	LM1	0	
7	High air gap measurement value	LM2	0	
8	Parity bit	P	Current calculation	Always an even number

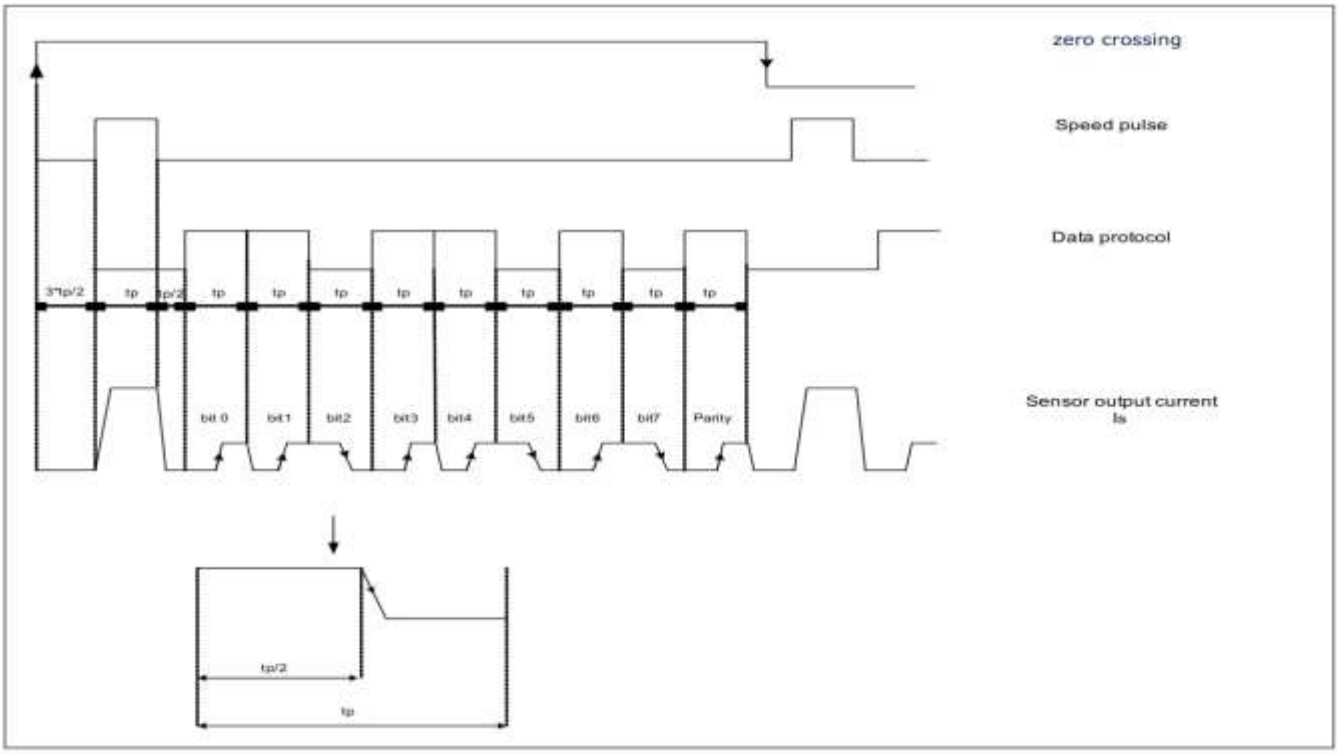


Figure 7-2 Manchester coding rules

7.1 Normal speed protocol

At normal speed (signal frequency less than 1800Hz), all data bits are output. At the beginning, the initial bit (ILOW) is sent as tp/2. Then a speed pulse with a duration of tp is emitted, followed by a current ILOW level of tp/2. Then send the data protocol. As shown in Figure 7-3

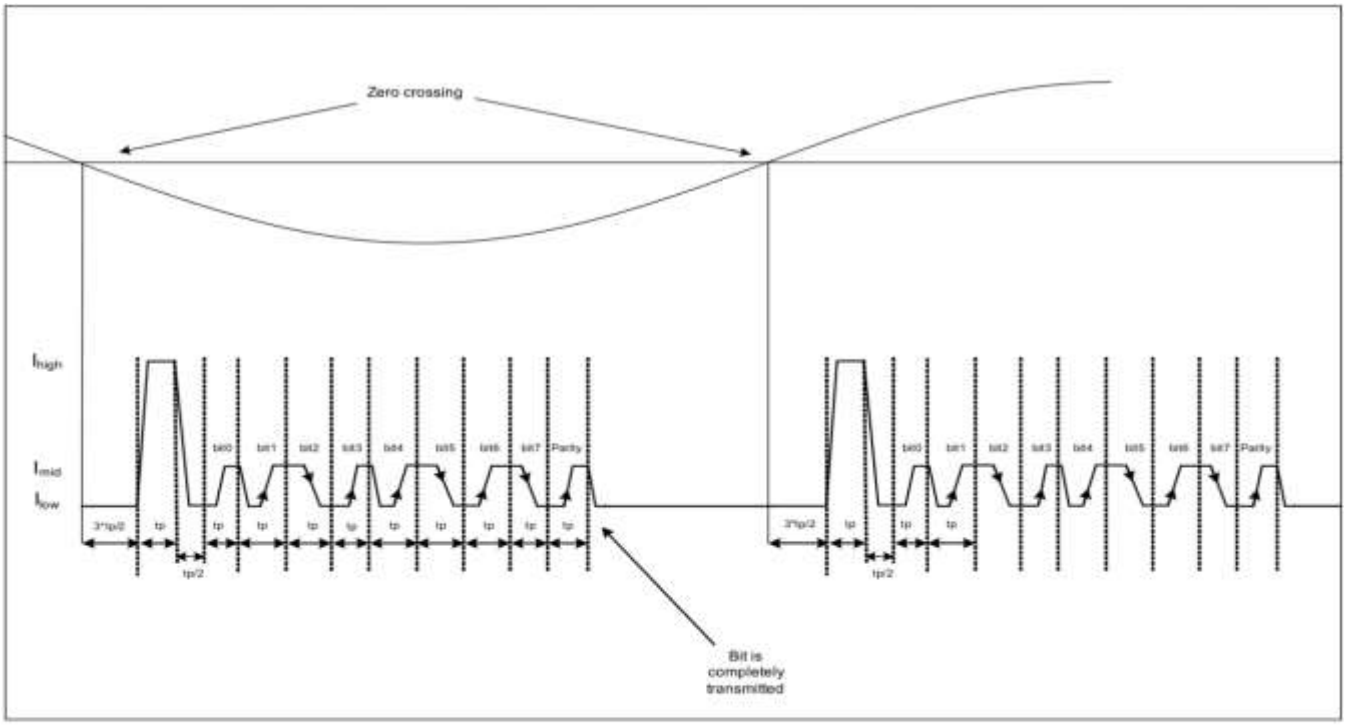


Figure 7-3 Normal Speed Protocol

7.2 High speed protocol

For higher speeds, the data protocol is shortened (the last bit is cut off). The following table shows the number of bits transmitted at different signal frequencies. The serial data protocol is shortened at high speeds because the time to reach the next speed pulse is shorter than the protocol period. Therefore, the last data bit is' cut off '. The maximum possible number of bits of additional information transmitted within each speed range. The output of the partially transmitted bits, known as' bit residues', is suppressed. The shortening of the protocol will not result in any 'bit residue' (incomplete transmission of bits). This means that the bits affected by the shortening will be fully transmitted in any case, which means that the bits that have already started must also be transmitted to the end. What must be output is not the bit affected by the shortening, but the current ILOW level. In all speed ranges and normal operating states of the sensor, that is, in the stationary protocol, the suppression of bit residuals does indeed work reliably. This ensures that there will be no compatibility issues under any normal operating conditions, such as EMC. Data transmission bit corresponding speed frequency:

	Speed signal frequency	Number of transmitted bits (data bits)
1	<1818Hz(1800Hz)	9（bit0-bit8）
2	<2000Hz(2000Hz)	8（bit0-bit7）
3	<2222Hz(2200Hz)	7（bit0-bit6）
4	<2500Hz(2400Hz)	6（bit0-bit5）
5	<2857Hz(2800Hz)	5（bit0-bit4）
6	<3333Hz(3200Hz)	4（bit0-bit3）
7	<4000Hz(4000Hz)	3（bit0-bit2）
8	<5000Hz(5000Hz)	2（bit0-bit1）

Note: The frequency of the electrical signal is twice the frequency of the magnetic field, and the frequency in parentheses is the specification of the AK protocol.

7.3 Static Data Protocol

If no increment is recognized within the time limit of tstop, the IC starts sending the static protocol. This protocol is sent every 150ms ± 20%. In this protocol, the current value of the speed pulse is set to Imid, and all other bits are transmitted as described earlier. For very slow wheel speeds, more than one stationary protocol can be issued between consecutive speed pulses.

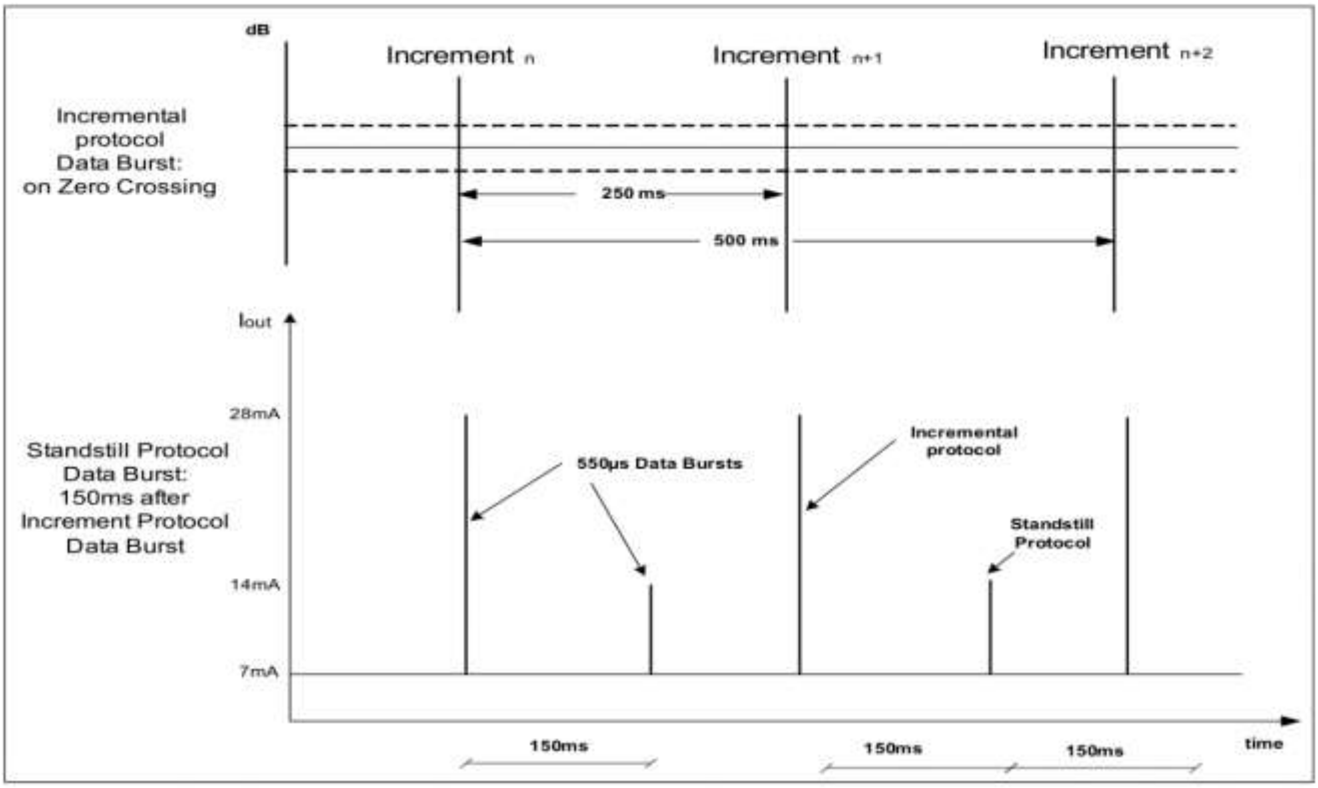


Figure 7-4 Static state output

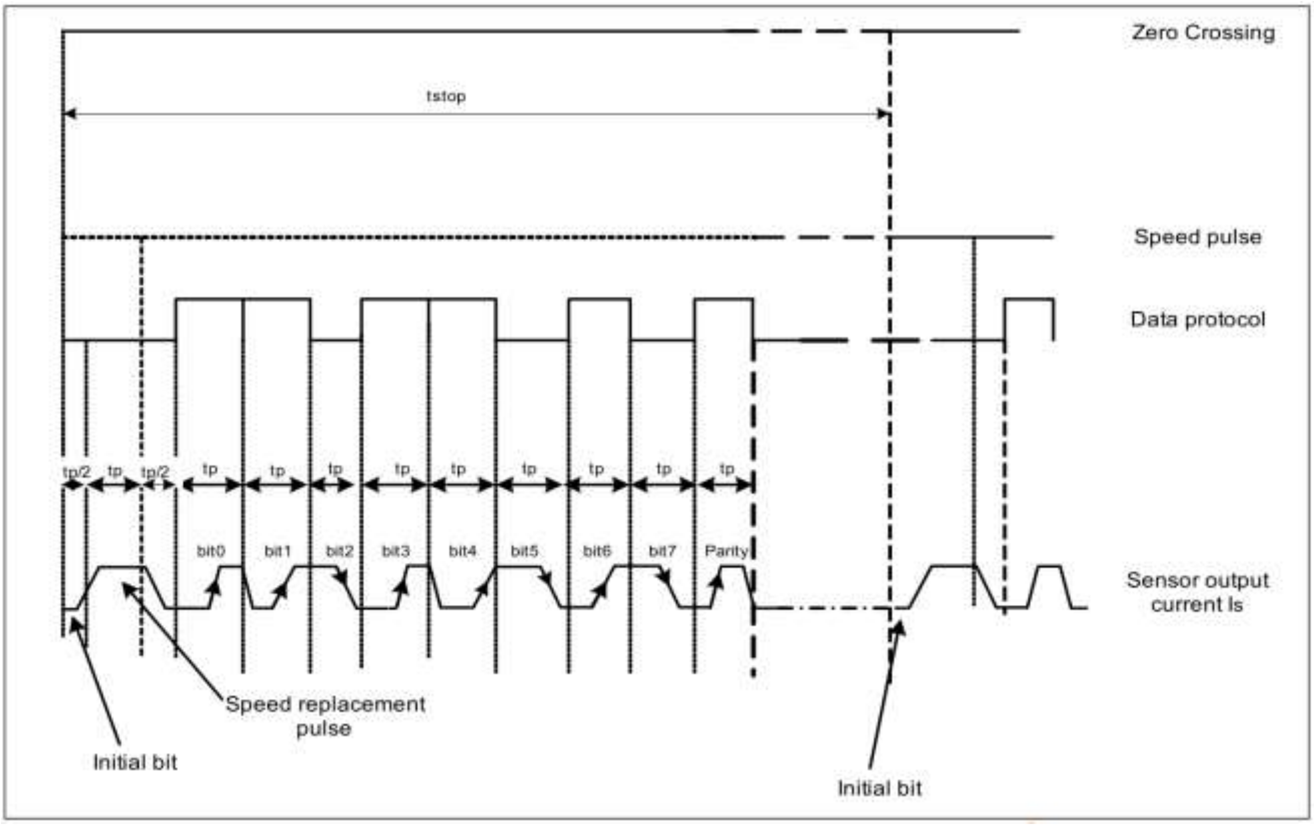


Figure 7-5 Static Data Protocol

Notes on the transition from stationary to moving:

If an increment of the magnetic encoder is detected, the static protocol will be terminated. The speed pulse IHIGH has priority over the initial position (ILOW). Due to the need to suppress "bit residues" in static protocols, protocol slicing can only occur between two data bits, rather than during ongoing bit transfers. The initial position always has a low current ILOW before the velocity pulse, with a duration of at least tp/2. As shown in Figure 7-6, this helps the ECU (Electronic Control Unit) detect speed pulses.

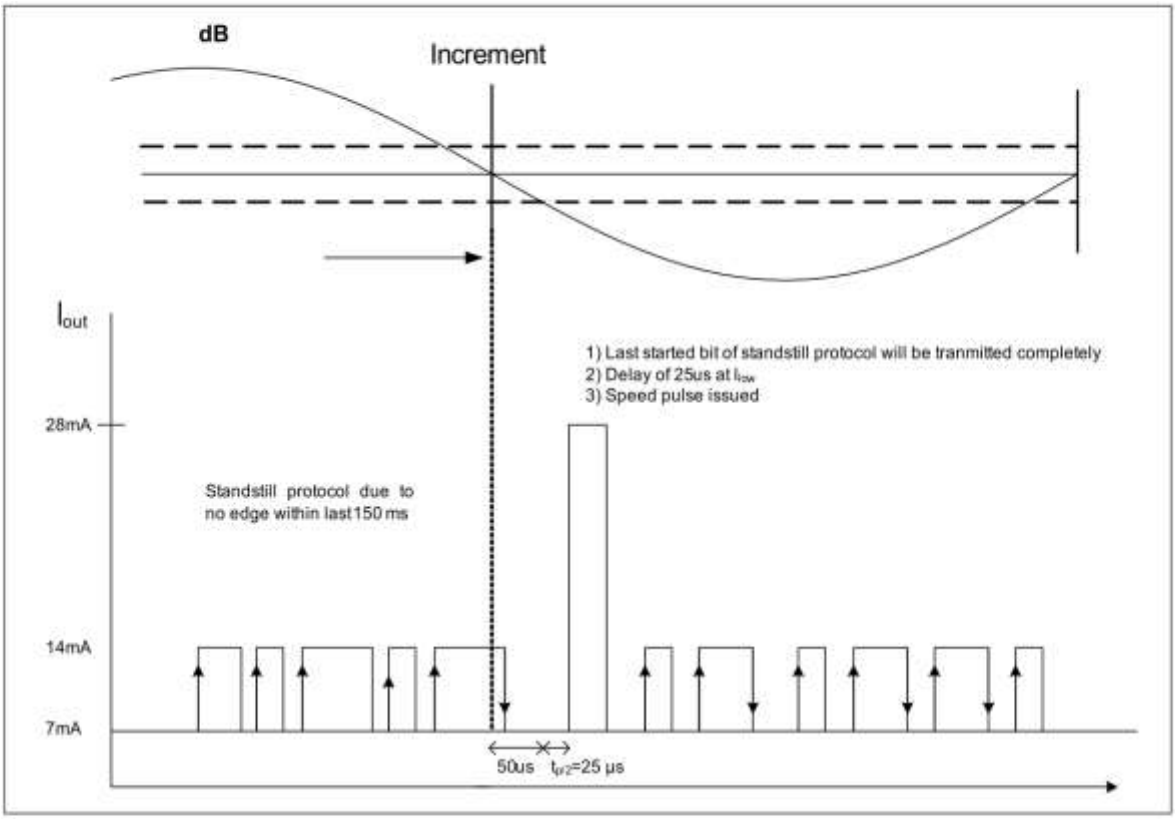


Figure 7-6 Using residual bits to suppress the motion of the starting wheel in a static protocol

Handling of "validity of direction" and "direction" under static protocol:

In any stationary state, DR transmits with zero (default value) and GDR transmits with invalid (=0). When the first 5 stationary protocols appear consecutively, the direction algorithm is reset. Therefore, direction detection and direction change detection are performed at the next three zero crossings (velocity pulses) (GDR=invalid, DR=default), GDR is valid, and the corresponding direction is output at the third velocity pulse after being stationary.

Processing of "Validity of Magnetic Field Strength Measurement Signal" in Static Protocol:

In the static protocol, the validity of signal measurement (SLM) is sent as 1 (invalid), and the signal amplitude (level related to LR) is sent as 0. If the first 5 stationary protocols occur consecutively, reset SLM/LM to invalid. SLM remains invalid until two new extreme values in dB are found. Based on the amplitude of dB and the phase of the stationary protocol, SLM is effective in the 2nd, 3rd, or 4th velocity protocol after every 5 stationary protocols.

Handling of error bit "air gap reservation" (=LR bit) in static protocol:

Transmit with '0' (no errors) in a static protocol. When the first 5 stationary protocols occur consecutively, the value is reset to 0. The static protocol LR remains' 0 '(error free) until two new extremum values are found in dB. The initial position always has a low current ILOW before the velocity pulse, with a duration of at least tp/2. This helps the ECU detect speed pulses.

7.4 Bit Stump suppression

Bit Stump technology is a strategy implemented in wheel speed sensors to prevent the phenomenon of "position stakes". Bit stake usually refers to the phenomenon of sudden interruption of data bits caused by incomplete transmission of sensor output signals during high-speed changes.

This inhibition method is based on the following principles:

1. Constant time offset of output signal: When a new data protocol starts, the sensor's output will always be delayed by one bit time tp. This is equivalent to adding a time offset to the output signal, and its effect is as follows:

2. Prevent premature start of the initial bit: When a new protocol starts, the first data bit will not be immediately started to prevent the generation of bit stakes during the ongoing data protocol during high-speed driving. On the contrary, the system will first wait for the time offset tp and continuously monitor the output of the previous ongoing protocol during this period. If it is found that the bit output of the previous protocol is still active, the bit will be fully transmitted instead of being disconnected, effectively preventing the occurrence of bit stubs.

3. Suppress possible subsequent data bits: During this offset time, suppression of the next possible data bit from the previous protocol will be introduced to ensure the completion of the current bit transmission and prevent further bit transmission (i.e., the remaining bits from the previous protocol). When the offset time ends, the first bit of the new protocol begins to be transmitted.

4. Effectiveness under the idle protocol: Even if a new increment of the encoder is detected while the vehicle is stationary, resulting in bit transmission during the ongoing idle protocol, the current bit

transmission will not suddenly terminate and form a bit stake due to the new increment. Extra bits will be suppressed, and after a delay phase, new transmissions will begin after a time interval of tp/2, followed by normal transmission of speed pulses and data protocols.

In summary, the method described above achieves bit stub suppression by performing a constant time offset on the sensor output signal, ensuring the integrity of the data protocol and avoiding the occurrence of bit stub phenomenon, whether there is sufficient bit transmission time between continuous protocols or in high-speed dynamic changes or even idle states. The following examples will demonstrate the specific effects of this method in different scenarios.

The first scenario: Do not cut off the transmission of the previous protocol. In the wheel speed sensor, even if the time interval between the two protocols is long enough to transmit all data bits, a constant time offset tp strategy is still adopted when starting the new protocol at the incremental time of the new encoder. This means that when a new encoder position increment is detected, the sensor output will not immediately start the first bit transmission of the new protocol, but will first wait for a time tp as the offset. During this period, the system will monitor whether there are any unfinished bit outputs from the previous protocol. If there is an active bit output, the system will ensure that the bit is transmitted completely and accurately, effectively avoiding the occurrence of bit stubs. During this offset time tp, the possible next data bit of the previous protocol will also be suppressed to ensure that the current ongoing bit transmission is completed completely and to prevent any unnecessary bit transmission from the previous protocol. After waiting for the end of the TP time, the new protocol will start transmitting its first bit, which has a width of tp/2, followed by the transmission of speed pulse signals and other protocol related data. The advantage of this design is that it not only effectively prevents residual bits at normal speeds, but also ensures that the currently ongoing bit transmission is not accidentally interrupted even during stationary protocol periods (such as sudden detection of new encoder increments when the vehicle is stopped), thereby maintaining the integrity of data transmission.

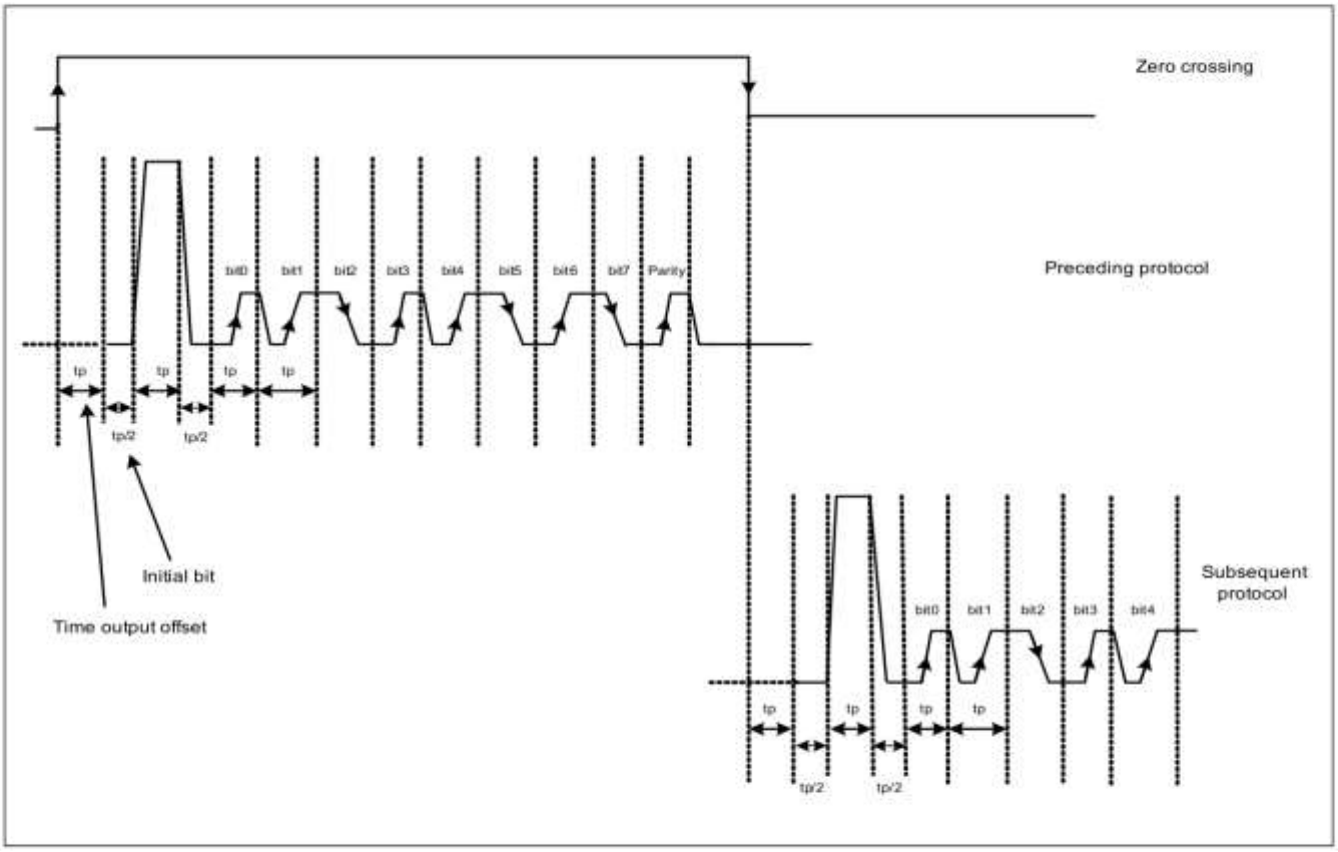


Figure 7-7 First scenario

The second scenario: the last bit of the previous protocol is cut off.

When the time interval between two consecutive protocols is no longer sufficient and a new increment of the encoder appears, it happens to be in the process of the last bit of the previous protocol still being transmitted.

At this point, the new protocol will also start following the rule of a constant time offset tp. However, the sensor will now recognize that a bit transmission is still in progress.

In this case, the current output offset time will ensure that the incomplete transmission bit is fully transmitted. After the output offset time ends, the new protocol will start transmitting its initial bits (with a width of tp/2) as planned, followed by velocity pulses and other protocol content.

In this way, even in emergency situations, it can be ensured that no bit information is lost and a new protocol transmission can be smoothly started, effectively avoiding the occurrence of bit stub phenomenon.

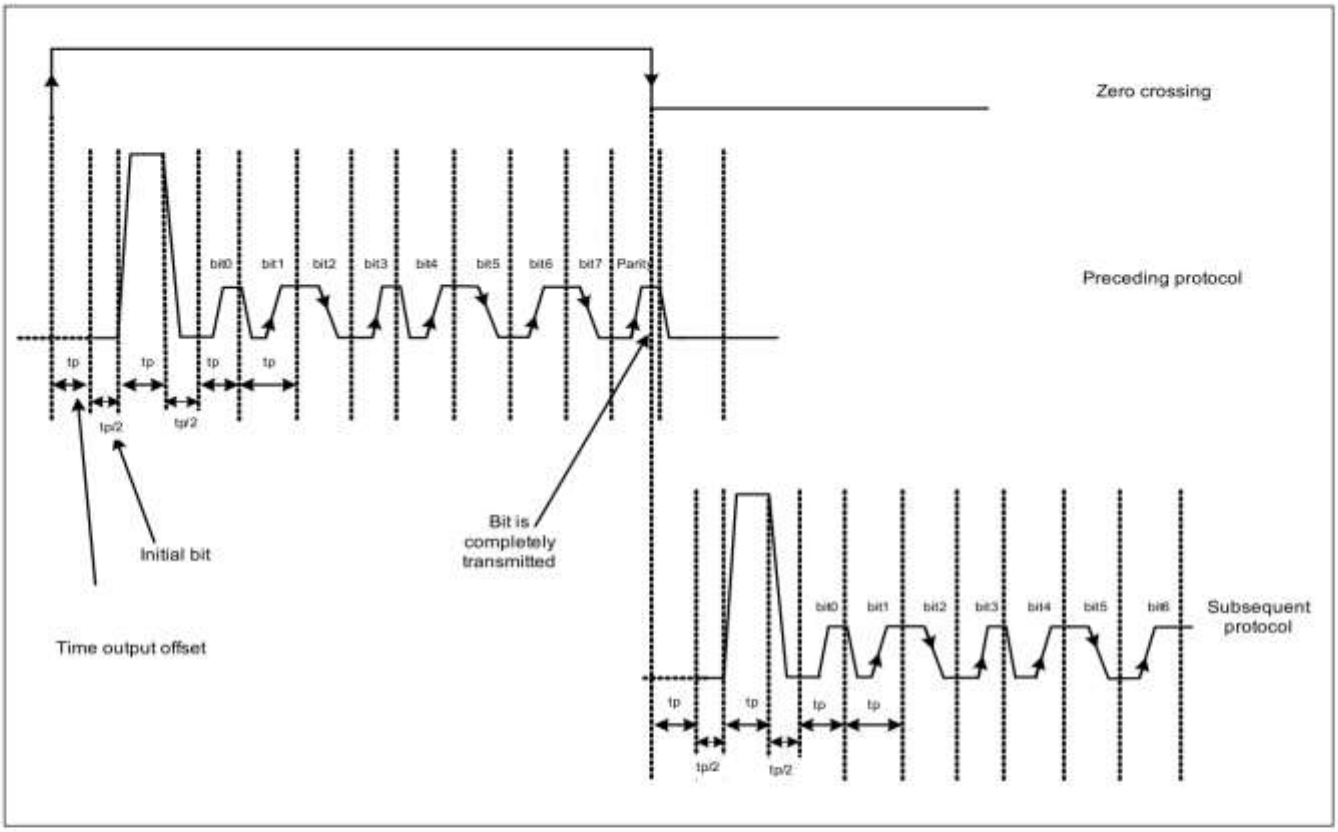


Figure 7-8 Second scenario

The third scenario: Several bits of the previous protocol are cut off.

When the encoder detects a new incremental value, such as during the transmission of the 6th bit in the previous protocol. At this moment, the new protocol will also restart with a constant time output offset tp. The sensor will recognize that there is still bit transmission in progress.

Therefore, within the current output time offset, the 6th bit of the previous protocol will be fully transmitted. In addition, the 7th and 8th bits (check bits) that should be transmitted but have not yet been sent in the original protocol will be suppressed and will no longer be transmitted. The line is restored to a clean state again. After the output time offset ends, according to convention, the initial bit (with a width of tp/2) is transmitted first, followed by other protocol contents such as speed pulses.

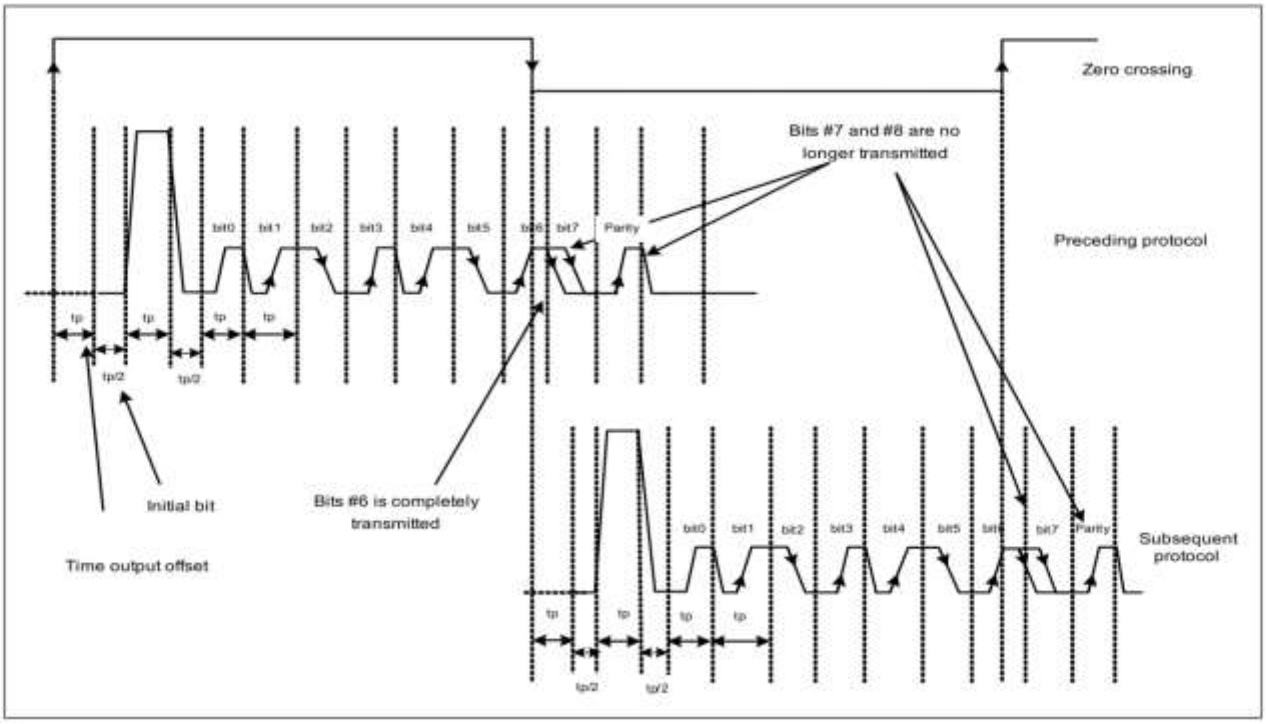


Figure 7-9 Third scenario

7.5 Operation mode and status

The basic job of AH743C is to measure the differential magnetic field of the rotating target wheel and generate an output signal that represents the wheel speed and provides information about the direction of rotation and signal quality. This integrated circuit has a three-level current interface. The function of AH743C can be divided into two different stages: uncalibrated and calibrated mode.

After the initial calibration delay time td input, the differential magnetic signal dB is tracked by an analog-to-digital converter (ADC) and monitored in a digital circuit. In order to detect, the signal needs to exceed the internal threshold DNC (Digital Noise Constant). When the signal slope is identified as a falling (or rising) edge and the signal change exceeds DNC, locate the first extremum and trigger the first output pulse. The constant value of digital noise varies with the amplitude of the magnetic field, resulting in a change in the phase shift between the magnetic input signal and the output signal. The value of the digital noise constant is determined by the signal amplitude. The first DNC (2 × dB limit) is shown by the arrows in Figure 5-7. When the signal changes again beyond the new DNC (calculated by (min1+max1)/2) at the next rising (respectively falling) edge, the second output is triggered. When the maximum and minimum values are found, offset correction will be performed. This causes a phase shift in the output signal and the sensor enters calibration mode. In calibration mode, the switch is triggered by the zero crossing of the differential magnetic signal. Reduce the minimum/maximum detection to 1/4 of the peak to peak ratio. In calibration mode, the minimum DNC is 2 times the dB limit. The nominal delay of the continuous speed pulse here is approximately 180°.

Processing additional information bits in uncalibrated and calibrated modes:

Signal amplitude measurement: If two valid extreme values are found, SLM is valid (the first extreme value after power on is invalid). The latest SLM with the fourth protocol is valid.

High frequency startup may lead to protocol shortening. Perform bit suppression in the chapter "7.4 Bit Stump Suppression".

The direction signal is always sampled by the main comparator switch (75us ± 25%) before the sensor output switch (speed protocol). After two consecutive samples of the directional signal, calculate the offset of the directional signal, and then compare the third sample with the offset. The direction is given by the sign of the third sampling direction signal and the direction of the edge (rising or falling) of the magnetic velocity signal. Using this direction detection method, the detected direction is most effective under the 4th output speed protocol. The GDR bit provides information on whether the detected direction is valid. On AH743C, if the difference between two consecutive samples of the direction signal (also used to calculate direction) is greater than twice the dB limit and the speed signal is greater than four times the dB limit, direction detection is effective, as shown in Figure 7-10.

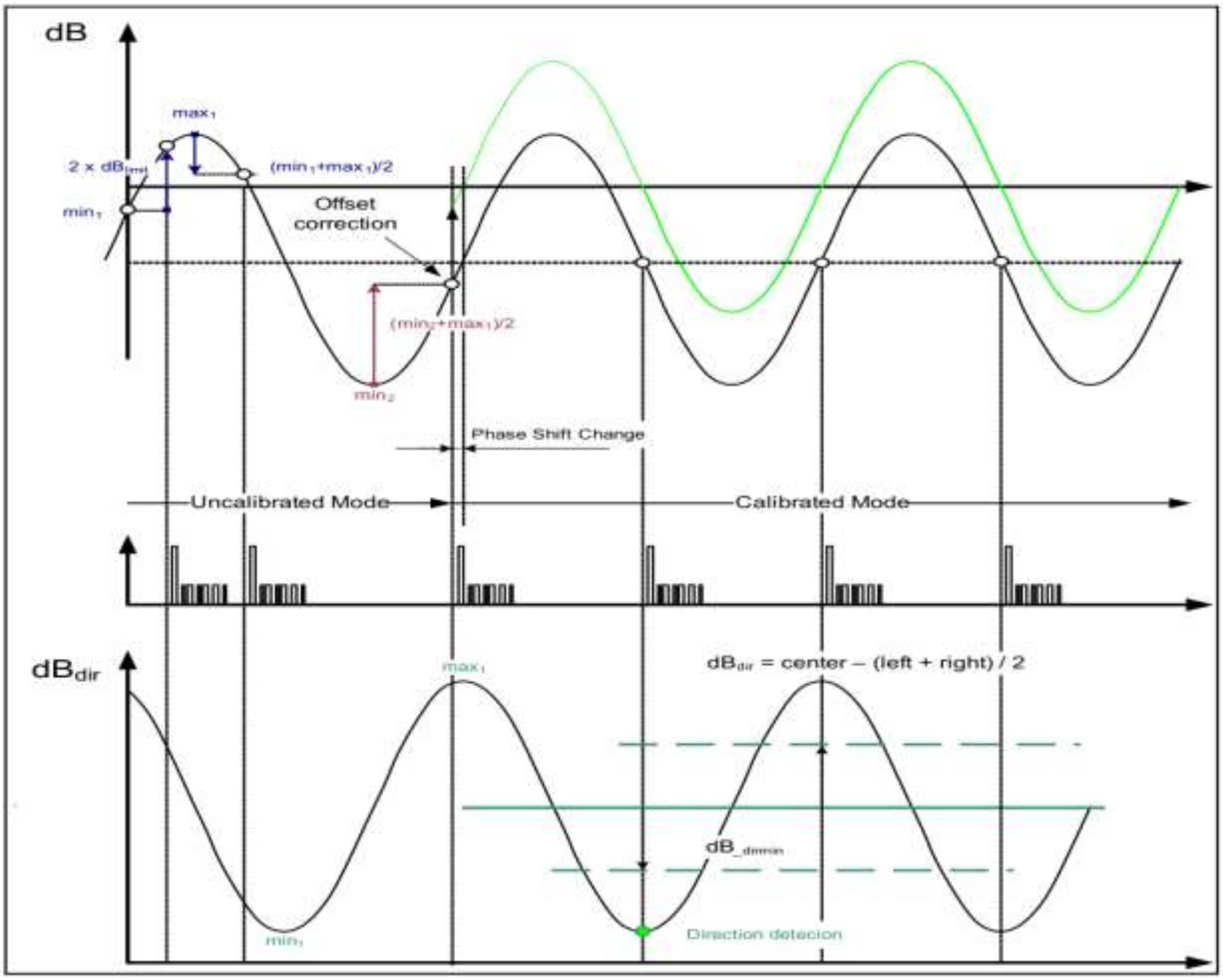


Figure 7-10 Direction detection

7.6 Power on and undervoltage states

The voltage supply comparator has an integrated hysteresis Vhys, which releases the maximum value of the voltage level Vrel. This determines the minimum power supply voltage VDD required for the chip. The minimum hysteresis Vhys has been achieved, thereby avoiding output switching caused by additional voltage drop at RM when switching from low current level to high current level at VDD=4.5V when the power supply voltage VDD is modulated (designed for RM=50 Ω). As long as VDD does not exceed Vrel, the sensor remains at a low level (V_{DD}>Vres).

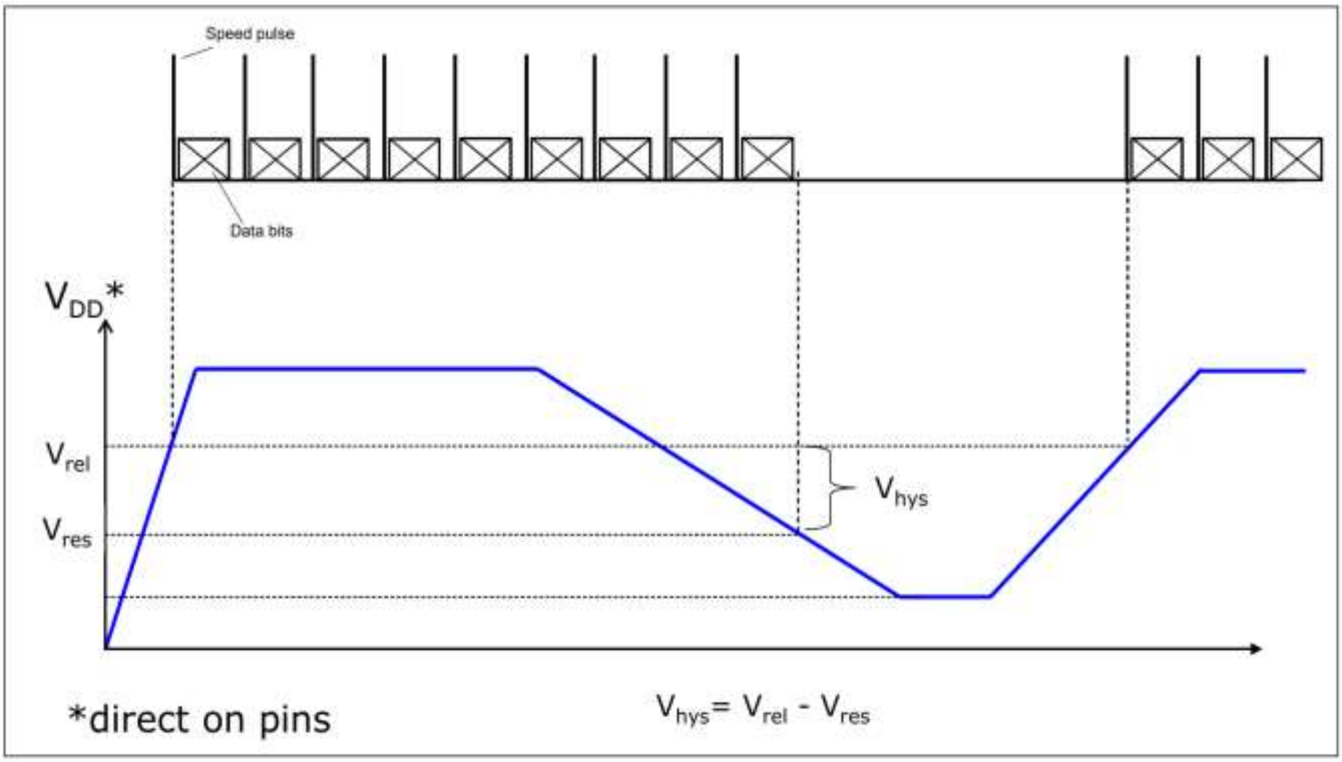


Figure 7-11 Startup and undervoltage states

8. Absolute limit parameter

Exceeding the limit parameters during use can lead to unstable chip functionality, and prolonged exposure to this environment can damage the chip. Tj = -40℃ to 150℃, 4.5V≤VDD≤16.5V.

Symbol	Parameter	Min	Max	Unit	Condition
V_{DD}	Power supply Voltage	-0.3		V	Tj<80℃
			16.5	V	Tj=170℃
			20	V	Tj=150℃
			22	V	Tj=150℃ t=10×5min
			24	V	t=10×5min R_M≥50Ω included in V_{DD}
			26	V	t=400ms, R_M≥50Ω included in V_{DD}
Urev	Reverse voltage	-16		V	t<1h，R_M≥55Ω included in V_{DD}
Irev	Reverse polarity current		200	mA	External current limitation required, t < 4 h
Tj	Junction temperature	−40−	110		125000h,V_{DD}<16.5V
			125		10000h,V_{DD}<16.5V

			150		5000h,V_{DD}<16.5V
		–	160		2500h,V_{DD} <16.5V
		–	170		500h,V_{DD}<16.5V
		–	190		4h,V_{DD} <16.5V
T_A	Operating ambient temperature	-40	150	℃	
V_{ESD}	Antistatic capacity	-	±12	kV	AEC-Q100

9. Electrical characteristic

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating voltage	V_{DD}	6.5	--	20	V	Excluding RM resistors
V_{DD} hysteresis	Vres	4.0	4.2	4.5	V	AK: Reset voltage
	Vhys	1.6	1.8	2.3	V	
	Vrel	5.8		6.5	V	AK: recovery voltage
Operating current (low)	I_{LOW}	5.9	7	8.4	mA	
Operating current(Middle)	I_{MID}	11.8	14	16.8	mA	
Operating current (high)	I_{HIGH}	23.6	28	33.6	mA	
Working current ratio	I_{MID}/I_{LOW}	1.8	2	2.6		Figure 9-1
Working current ratio	I_{HIGH}/I_{LOW}	3.6	4	5.0		Figure 9-1
Output swing rate	t_r(rise)	8		26	mA/µs	R_M = 50 Ω +/-5% Figure 10-1
	t_f(down)	8		26	mA/µs	R_M = 50 Ω +/-5% Figure 9-1
linearity	dI/dV_{DD}			90	µA/V	
Initial calibration delay	$t_{d,input}$		220	300	µs	
Power-on time u	t_{pu}			1	ms	
Initial calibration time	td_input		220	300	µs	
Duty cycle	DC	40	50	60	%	
Signal frequency	f	1		5000	Hz	
Signal Jitter 1Hz<f<2500Hz	$S_{Jit\text{-}close}$			±2	%	1σ value V_{DD}=12 V $\Delta B \geq 2$ mT

Signal Jitter 2500 Hz < f < 10000 Hz	$S_{Jit\text{-}close}$			±3	%	1σ value V_{DD}=12 V ΔB ≥ 2 mT

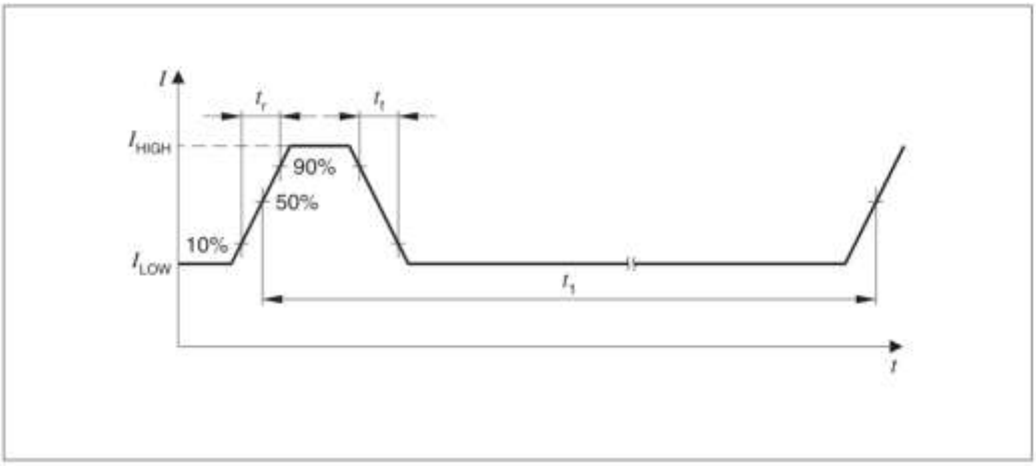


Figure 9-1 Definition of Signal Rise Time tr and Fall Time tf

The amplitude (Δ I) refers to the 80% positive and negative sides of Ilow to Imid and Ilow to Ihigh, and vice versa. The slew rate is calculated by dividing by Δ I/t r (rise time) or Δ I/t f (fall time).

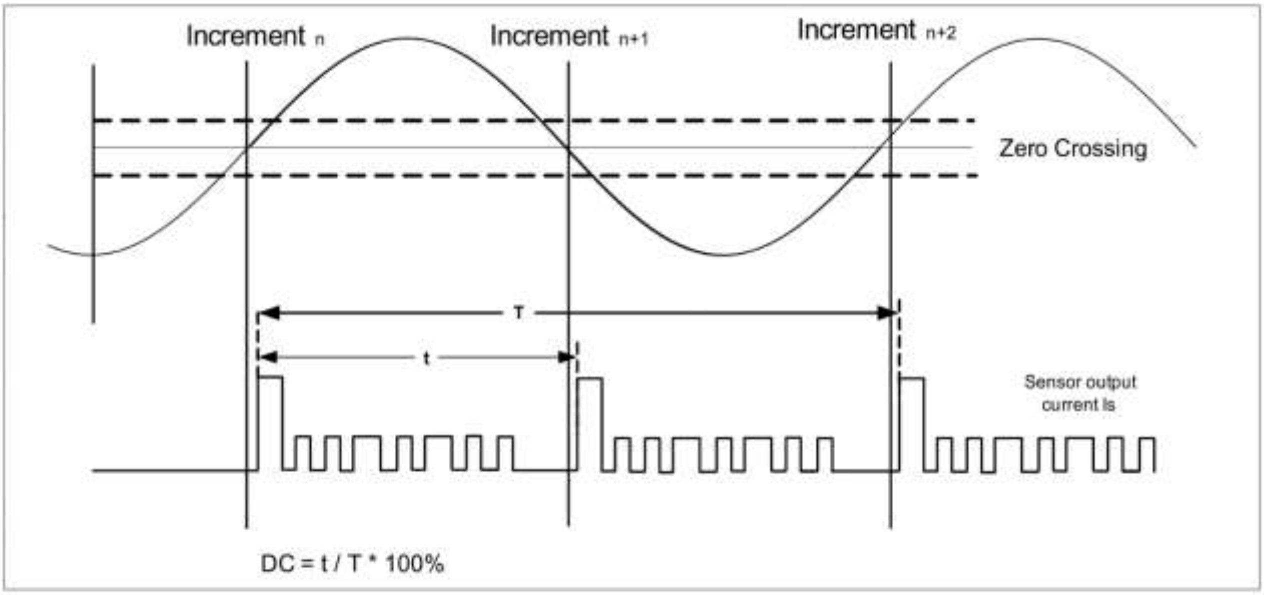


Figure 9-2 Definition of Signal Duty Cycle

10. Temporal characteristic

Unless otherwise specified, the following parameters are tested under constant amplitude and bias of the input signal (test conditions are V_{DD}=12V, T_A=25 ℃, circuit reference test circuit diagram 10-1).

Symbol	Parameter	description	Min	Typ	Max	Unit
tp	Pulse width of speed pulse	Figure 7-2	38	45	52	µs

tp	Pulse width of data bits	Figure 7-2	38	45	52	μs
tstop	rest time	Figure 7-5	76	90	104	ms
tp/2	Pulse width of initial position	Figure 7-2	153	180	207	μs

11. Magnetic field characteristic

Unless otherwise specified, the following parameters are tested under constant amplitude and bias of the input signal (test conditions are V_{DD}=12V, T_A=25°C, circuit reference test circuit Figure 11- 1).

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Pre-induction	B_0	-500	-	+500	mT	
Limit threshold	ΔBLimit	0.35	0.8	1.34	mT	
Pre-induction offset between outer probes	$\Delta B_{stat., l/r}$	-30		+30	mT	
Differential induction	ΔB	-120		+120	mT	f=1kHz, Bdiff=5mT
Limit threshold drift limit range	ΔBLR	-5		+3	%	Additional drift of the same sensor during its lifespan at25 ° C
		1.02	1.6	2.18	mT	
The effectiveness of magnetic field strength measurement	SLM					'0'=valid, invalid under voltage, initial value after power on
Magnetic field strength (relative to LR level)	LM =0	<0.8	<=1	<=1.2		
	LM =1	>0.8	>1	>1.2		
	LM =2	>1.48	>1.75	>2.1		
	LM =3	>2.5	>2.95	>3.6		
	LM =4	>4.2	>4.95	>6.0		
	LM =5	>7.0	>8.25	>9.9		
	LM =6	>12.0	>14.2	>17.1		
	LM =7	>21.0	>24.7	>29.7		

12. Reference circuit

12.1 Test Circuit

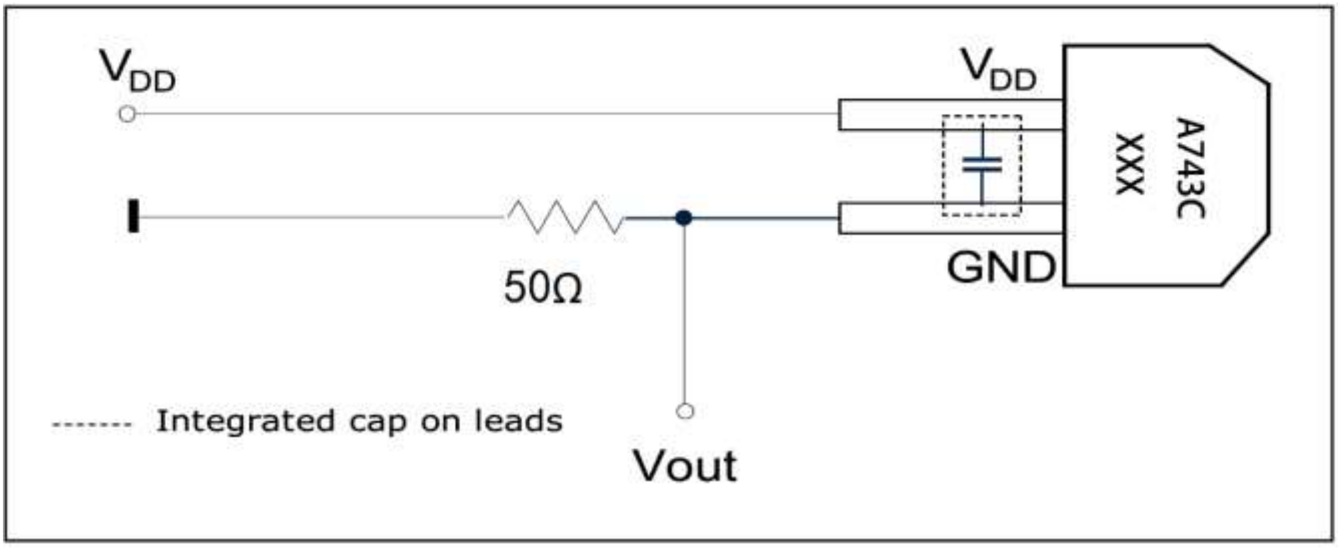
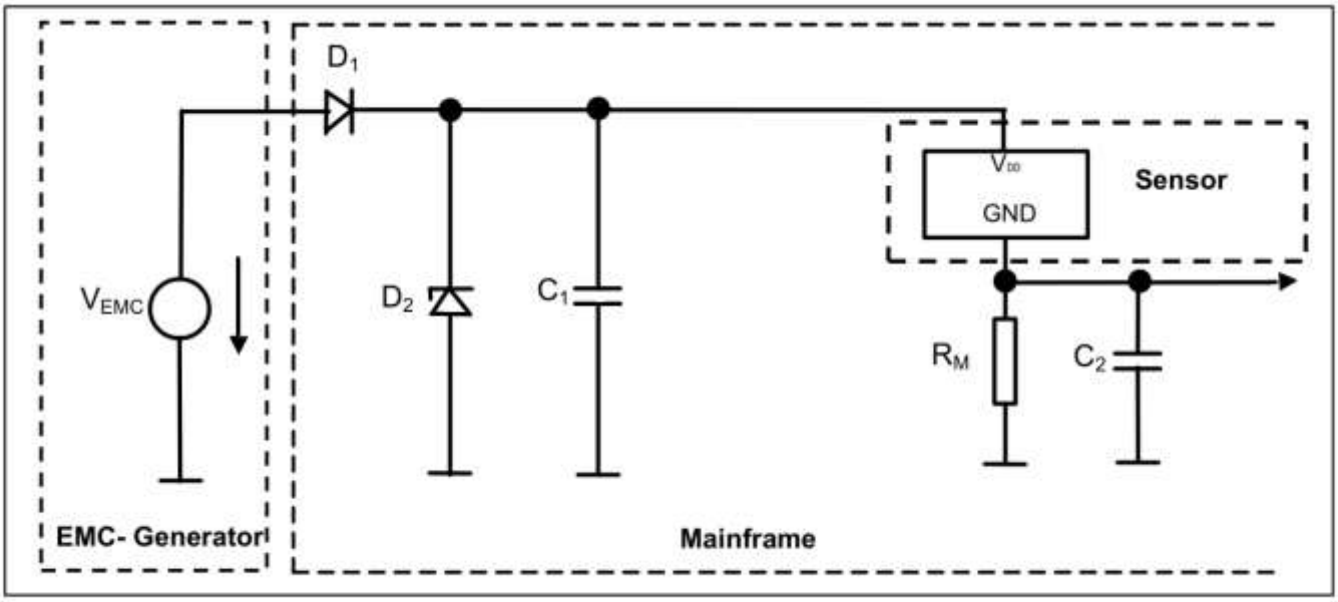


Figure 12-1 Test Circuit

12.2 Application reference circuit

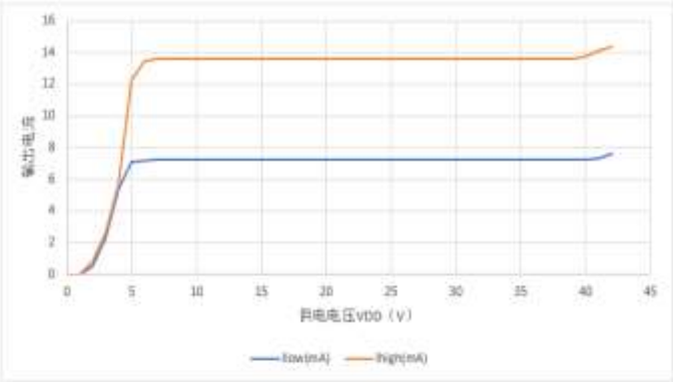


Components:	D1:	1N4007
	D2:	T 5Z27 1J
	C1:	10µF/35V
	C2:	1nF/1000V
	RM:	50Ω/5W

Figure 12- 2 Application reference circuit

13. Characteristic curve

Performance characteristic test (test circuit diagram 12-1)



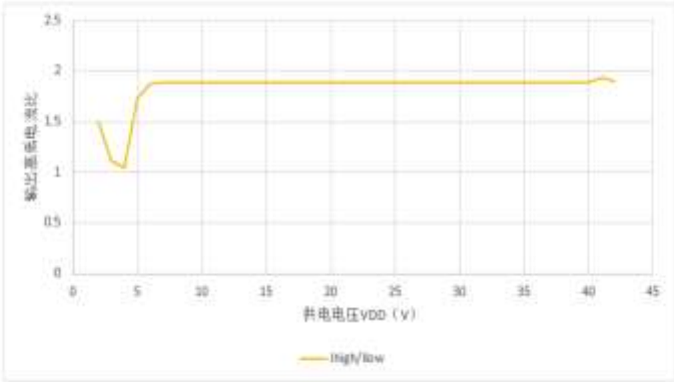
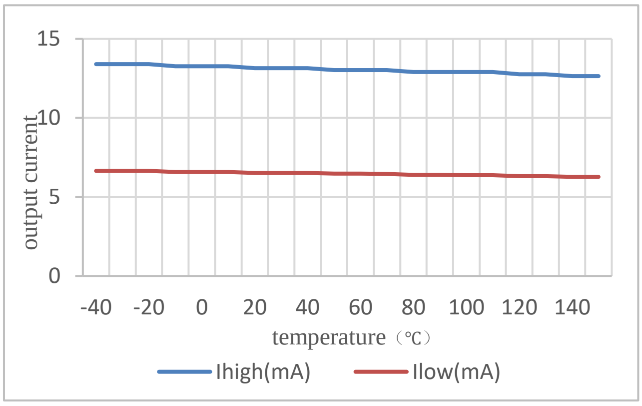


Figure 13-1 Working current and current ratio under voltage of 0-42V



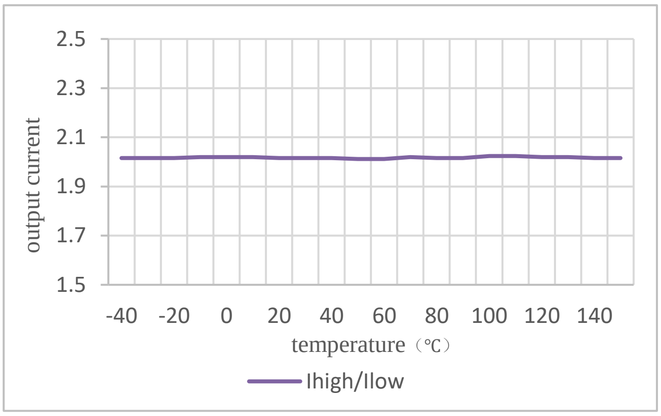


Figure 13-2 -40 to +150 °C Operating current and current ratio

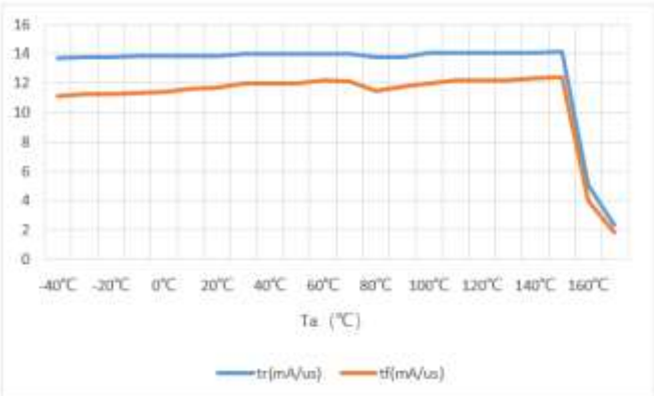


Figure 13-3Output signal slew rate at -40~+150 °C

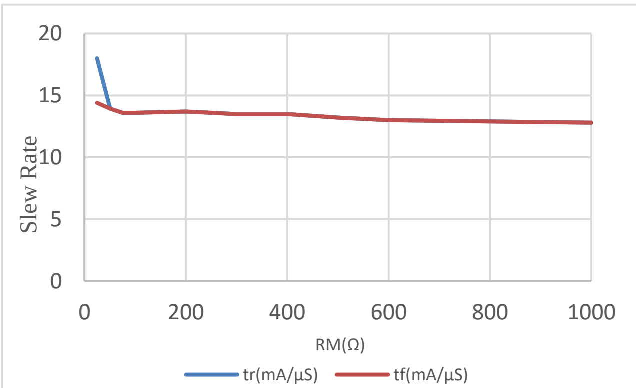
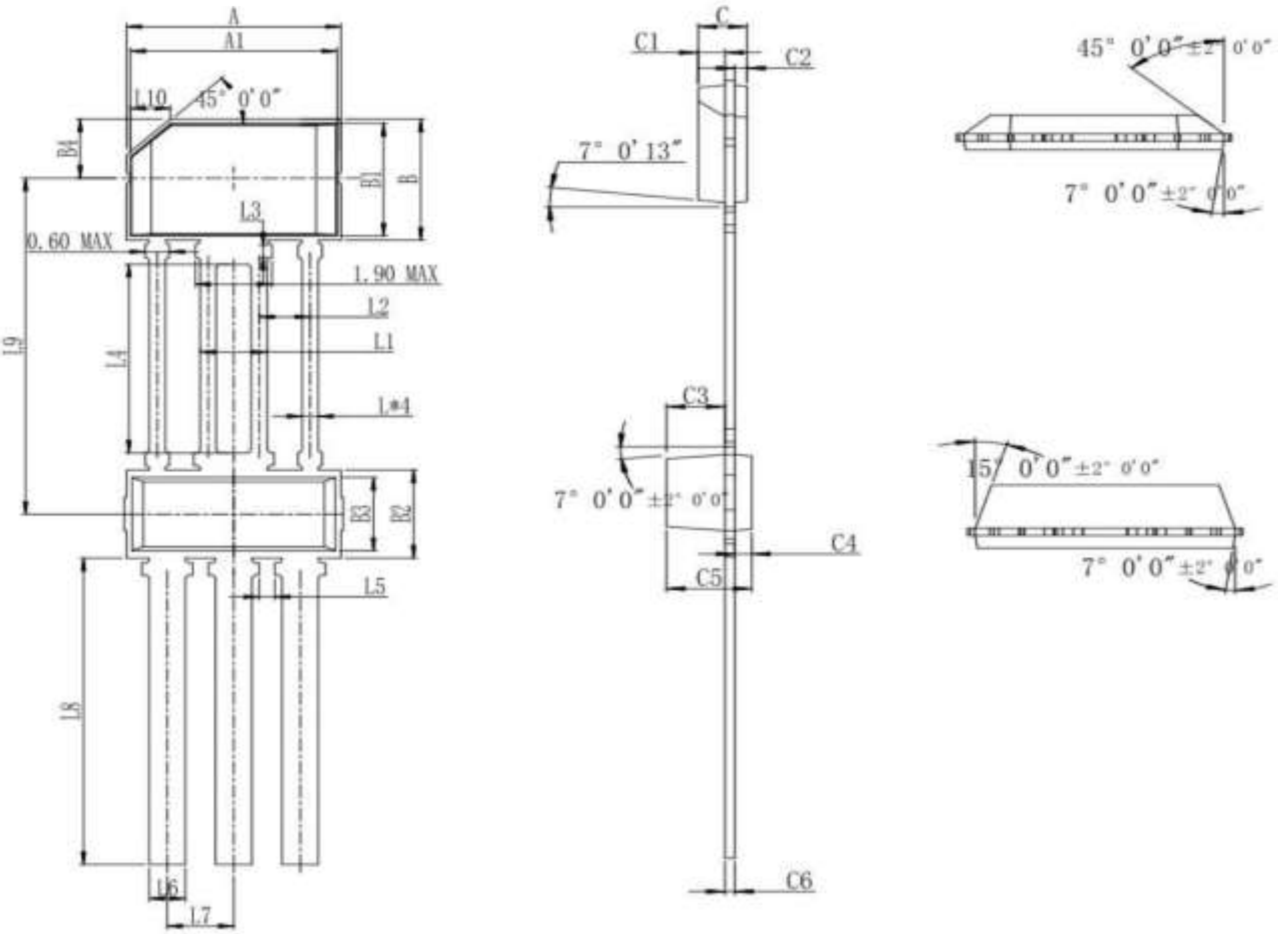


Figure 13-4 RM (1~1000) output signal slew rate

14. Package information



15.Note

- Hall chips are sensitive devices, and electrostatic protection measures should be taken during use, installation, and storage.
- During installation and use, mechanical stress applied to the device casing and leads should be minimized as much as possible.
- It is recommended that the welding temperature should not exceed 350 ℃ and the duration should not exceed 5 seconds.
- To ensure the safety and stability of Hall chips, it is not recommended to use them beyond the parameter range for a long time.

16. Historical Version

No.	Time	Describe
1	February.024	Publish
2	April,2024	Update description ambiguity
3	April,2024	Revise the layout